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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/432,855	11/02/1999	DESMOND E. WONG	0100.9901360	1672

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EXAMINER	
SHANKAR, VIJAY	

ART UNIT	PAPER NUMBER
2629	

MAIL DATE	DELIVERY MODE
10/16/2007	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	09/432,855	WONG, DESMOND E.	
	Examiner	Art Unit	
	VIJAY SHANKAR	2629	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *08 August 2007*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-6,10-13 and 23-27* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-5,10-13 and 23-27* is/are rejected.

7)☒ Claim(s) *6* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

1. Applicant's request for reconsideration of the finality of the rejection of the last Office action is persuasive and, therefore, the finality of that action date 2/20/07 is withdrawn.

Claim Rejections - 35 USC § 103

2. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

3. Claims 1-5,10-13 and 23-27 are rejected under 35 U.S.C. 103(a) as being unpatentable over Cho et al (5,798,951) in view of Stoye (5,969,696) .

Regarding Claim 1, Cho et al teaches a method for detecting a monitor (Fig.1), the method comprising: monitoring pin of a connector coupled to a flat panel (see element 60 in Fig.1) display (Figs. 1-2; Col.4, line 31- Col.5, line 66; Col.15, line 6- Col.16, line 65); asserting (Col.10, lines 5-40) an output signal to indicate the one pin is in a first state (fig.1; Col.3, lines 3-31; Col.5, lines 18- Col.6, line 30; Col.9, lines 17-37); and receiving the output signal at a display engine. (Figs. 1-4; Col.3, lines 3-31; Col.4, line 31- Col.5, line 66; Col.15, line 6- Col.16, line 65). However, Cho et al does not teach a method for detecting a monitor, the method comprising monitoring one pin of a connector coupled to a flat panel display.

Stoye teaches a method for detecting a monitor, the method comprising monitoring one pin (50 in fig.2; Column 3, lines 7-15) of a connector coupled to a flat panel display (see Column 2, line 6- Column 3, line 15) .

Thus, it would have been obvious to one of ordinary skill in the art at the time the invention was made to have incorporated the teaching of Stoye into Cho et al for recognizing the flat panel display.

Regarding Claims 2-4, 24, 26, Cho et al teaches a method wherein the output signal is an interrupt signal, the interrupt signal is a system interrupt for a general purpose computer, and the output signal is stored in a register. (Fig.3; Col.5, line 19-56).

Regarding Claims 5, 27, Cho et al teaches the method further comprising determining if a voltage level of the one pin is in a stable state before asserting the output signal (Fig.3; Col.5, line 5-66; Col.10, lines 4-40; Col.11, line 31-Col.12, line 56).

Regarding Claims 10-13, Cho et al teaches the method further comprising the step of: operating in a normal mode of operation prior to monitoring, wherein the one pin is in a second state, and the first state is indicative of a flat panel display being coupled and decoupled to the connector, and driving the flat panel display from the flat panel display engine in response to asserting (Col.10, lines 5-40)

the first output signal. (Figs. 1-4; Col.3, lines 3-31; Col.4, line 31- Col.5, line 66; Col.15, line 6- Col.16, line 65).

Regarding Claim 23, Cho et al teaches a system for providing a display image to a flat panel monitor (see element 60 in Fig.1), the system comprising: a processing module; and memory operably coupled to the processing module, wherein in the memory stores operational instructions that cause the processing module (fig.1; Col.3, lines 3-31; Col.5, lines 18- Col.6, line 30; Col.9, lines 17-37) to monitor pin of a connector coupled to a flat panel display (see element 60 in Fig.1) (Figs. 1-3; Col.3, lines 3-31; Col.4, line 31- Col.5, line 66; Col.15, line 6- Col.16, line 65); assert a output signal (Col.10, lines 5-40) to indicate the one pin is in a first state; and receive the output signal at a display engine. (Figs. 1-4; Col.3, lines 3-31; Col.4, line 31- Col.5, line 66; Col.15, line 6- Col.16, line 65). However, Cho et al does not teach a method for detecting a monitor, the method comprising monitoring one pin of a connector coupled to a flat panel display.

Stoye teaches a method for detecting a monitor, the method comprising monitoring one pin (50 in fig.2; Column 3, lines 7-15) of a connector coupled to a flat panel display (see Column 2, line 6- Column 3, line 15) .

Thus, it would have been obvious to one of ordinary skill in the art at the time the invention was made to have incorporated the teaching of Stoye into Cho et al for recognizing the flat panel display.

Regarding Claim 25, Cho et al teaches the method for detecting a monitor, the method comprising: providing display information to a first display, (fig.1; Col.3, lines 3-31; Col.5, lines 18- Col.6, line 30; Col.9, lines 17-37); determining when an external flat panel display becomes available, by monitoring pin of a connector coupled to a flat panel display (see element 60 in Fig.1) (Figs. 1-3; Col.3, lines 3-31; Col.4, line 31- Col.5, line 66; Col.15, line 6- Col.16, line 65); asserting an output signal to indicate the pin is in a first state (Col.10, lines 5-40); providing an interrupt signal in response to the asserted output signal (Fig.3; Col.5, line 19-56) , and providing display information to the external flat panel display (see element 60 in Fig.1) in response to the interrupt signal. (Figs. 1-4; Col.3, lines 3-31; Col.4, line 31- Col.5, line 66; Col.15, line 6- Col.16, line 65). However, Cho et al does not teach a method for detecting a monitor, the method comprising monitoring one pin of a connector coupled to a flat panel display.

Stoye teaches a method for detecting a monitor, the method comprising monitoring one pin (50 in fig.2; Column 3, lines 7-15) of a connector coupled to a flat panel display (see Column 2, line 6- Column 3, line 15) .

Thus, it would have been obvious to one of ordinary skill in the art at the time the invention was made to have incorporated the teaching of Stoye into Cho et al for recognizing the flat panel display.

4. Claim 6 is objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

5. Applicant's arguments with respect to claims 1-6,10-13 and 23-27 have been considered but are moot in view of the new ground(s) of rejection.

6. Any inquiry concerning this communication or earlier communications from the examiner should be directed to VIJAY SHANKAR whose telephone number is (571) 272-7682. The examiner can normally be reached on M-F 7:00 am - 4:30 pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, BIPIN SHALWALA can be reached on (571) 272-7681. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

VIJAY SHANKAR
Primary Examiner
Art Unit 2629

VS